



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,773	09/29/2003	Hung-Yu Chiu	0941-0848P	7558
2292	7590	04/14/2006	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			TOLEDO, FERNANDO L	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H/A

Office Action Summary

Application No.

10/671,773

Applicant(s)

CHIU ET AL.

Examiner

Fernando L. Toledo

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 January 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-22,24 and 25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12-22 is/are allowed.
- 6) ☒ Claim(s) 1,4-11,24 and 25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 10/242,773.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| <p>1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)</p> <p>2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)</p> <p>3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>20060131</u>.</p> | <p>4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.</p> <p>5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)</p> <p>6) <input type="checkbox"/> Other: _____.</p> |
|---|--|

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
2. Claims 1, 7, 8, 10, 11, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (U. S. patent 6,521,922 B1) in view of Wu (U. S. Patent 6,689,658 B2).

In re claim 1, Huang, in the U. S. patent 6,521,922 B1; figures 1 and 2 and related text discloses, providing several interconnect structures (34) forming a passivation structure (42) over the several interconnect structures (34) wherein the passivation structure includes a first dielectric layer 36 and a silicon-oxy-nitride (SiO_xN_y) layer (38); and forming a second dielectric layer 40 over the surface of the passivation structure (Figure 2); wherein the first dielectric is formed by depositing a HDP oxide over the interconnect structure with high density plasma chemical vapor deposition (HDPCVD), and the thickness of the first dielectric layer is substantially between 7,000 – 10,000 Å so as to perform passivation function (Column 2, Lines 35 – 43).

Huang discloses wherein the interconnect structures are of a conductive material. However, Huang does not specifically teaches whether the interconnect structures are made of metal.

Wu, in the U. S. Patent 6,689,658 B2 discloses a method of forming a flash memory device which discloses that the interconnect structures can be form of conductive materials such

Art Unit: 2823

as metal (Column 5, Lines 45 – 50) and forming a substantially planarized inter-layer dielectric layer covering several metal interconnect structure (Figure 2C).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the interconnect structures of Huang out of metal, since, as taught by Wu, the interconnect structures of a flash memory device can be formed out of metal.

3. In re claim 7, Huang discloses wherein the thickness of the silicon-oxy-nitride (SiO_xN_y) layer is between 4,000 to 7,000 Å (Column 2, Lines 55 – 57).

4. In re claim 8, Huang discloses, wherein the memory device is a flash memory device (Column 2, Lines 28 – 30).

5. In re claim 10, Huang discloses wherein the first dielectric layer is thicker than or equal to the silicon-oxy-nitride (SiO_xN_y) layer (Column 2, Lines 35 – 43 and 55 – 57).

6. In re claim 11, Huang discloses, wherein at least one of the first dielectric layer, the silicon-oxy-nitride (SiO_xN_y) layer, or the second dielectric layer comprises substantially planarized surface (Figure 2).

7. In re claim 24, Wu discloses wherein the substantially planarized inter-layer dielectric layer is made of hydrogen blocking material (Column 12, Lines 25 – 35).

8. In re claim 25, Huang discloses wherein further comprising forming a substantially planarized inter-layered dielectric covering the plurality of metal interconnect structures (Figure 2).

9. Claims 4 – 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang as applied to claims 1, 7, 8, 10, 11, 24 and 25 above, and further in view of Wolf and Tauber (Silicon Processing for the VLSI Era Volume 1: Process Technology).

In re claim 4, Huang discloses forming the PSG layer (Column 2, Lines 50 – 55).

Huang in view of Wu does not disclose forming the PSG layer by APCVD.

However, Wolf in the textbook Silicon Processing for the VLSI Era Volume 1: Process Technology discloses that APCVD processes are simple reactors, have fast deposition at low temperatures (Page 168, Table 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the PSG layer of Huang by APCVD since as taught by Wolf, APCVD processes are simple reactors, have fast deposition at low temperatures.

10. In re claim 5, Huang discloses wherein the second dielectric layer is between 8,000 and 10,000 Å (Column 2, Lines 50 – 55).

11. In re claim 6, Huang discloses wherein the SiO_xN_y layer is deposited.

Wolf discloses on page 161 that CVD processes are often selected over competing deposition techniques because they offer the following advantages: a) high purity; b) a great variety of chemical compositions can be deposited among others.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the SiO_xN_y layer of Huang by CVD, since as taught by Wolf, CVD processes are often selected over competing deposition techniques because they offer the following advantages: a) high purity; b) a great variety of chemical compositions can be deposited among others.

12. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Wu as applied to claims 1, 7, 8, 10, 11, 24 and 25 above, and further in view of Sung (U. S. patent 6,235,592 B1).

Huang discloses that the device is a memory device, such as an EEPROM.

Huang in view of Wu does not disclose that the memory device could be a mask ROM.

However, Sung, in the U. S. patent 6,235,592 B1; figures 1a – 3 and related text, discloses, that memory devices could be, among others EEPROM, PROM and mask ROM (Column 1, Lines 18 – 25).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to teach that the memory device of Huang could be a mask ROM, since as taught by Sung, memory devices include but are not limited to EEPROM, PROM and mask ROM.

Allowable Subject Matter

13. Claims 12 – 22 are allowed over the prior art of record.

Response to Arguments

14. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO**

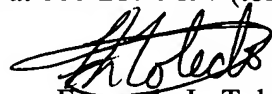
Art Unit: 2823

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando L. Toledo whose telephone number is 571-272-1867. The examiner can normally be reached on Mon-Fri 12pm-7:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Fernando L. Toledo
Patent Examiner
Art Unit 2823